

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:

GROUP: 2811

Takahiro KAWANO, et al.

SERIAL NO: 10/612,925

EXAMINER: NADAV, ORI

FILED: July 7, 2003

FOR: SEMICONDUCTOR DEVICE INCLUDING GATE WIRING, MAIN ELECTRODES AND CONNECTING PLATE CONNECTED ONTO SAID MAIN ELECTRODES

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

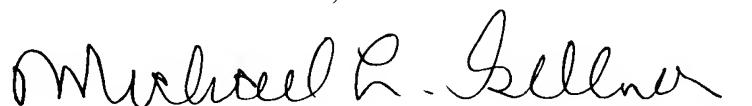
This request is being filed with a Notice of Appeal.

The review is requested for the reason(s) stated on the attached sheet(s). No more than five (5) pages are provided.

I am the attorney or agent of record.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.


Michael L. Gellner
Eckhard H. Kuesters
Registration No. 28,780

Customer Number

22850

Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 07/05)

Michael L. Gellner
Registration No. 27,256

DOCKET NO: 239801US2

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :
TAKAHIRO KAWANO, ET AL. : EXAMINER: NADAY, ORI
SERIAL NO: 10/612,925 :
FILED: JULY 7, 2003 : GROUP ART UNIT: 2811
FOR: SEMICONDUCTOR DEVICE :
INCLUDING GATE WIRING, MAIN :
ELECTRODES AND CONNECTING :
PLATE CONNECTED ONTO SAID MAIN :
ELECTRODES

PRE-APPEAL BRIEF REQUEST FOR REVIEW

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

REASONS FOR PATENTABILITY

In the outstanding Final rejection of June 2, 2008, Claims 1-2, 4-5, 45-47, and 52-71 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite; Claims 1-2, 4-5, 45-47, and 52-71 were rejected under 35 U.S.C. § 101 as inoperative and therefore lacking utility; and Claims 1-2, 4-5, 45-47, and 52-71 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sugawara et al. (U.S. Patent No. 6,342,709 B1, hereinafter “Sugawara”) in view of the Related Art of FIGs. 20 and 21.

SUGAWARA DOES NOT DISCLOSE OR RENDER OBVIOUS “A GATE WIRING WHICH IS FORMED ON THE SEMICONDUCTOR LAYER VIA A FIRST INSULATING FILM” AS RECITED IN CLAIM 1.

As depicted in FIG. 3, for example, in Sugawara, insulated gate electrode 14 is formed in the trench 69 after gate insulator film 9 is deposited on the inner surface of trench 69.¹ Sugawara describes a gate terminal TG connected to gate electrode 14.² Thus, there is no gate wiring described in Sugawara which is formed on the semiconductor layer via a first insulating film as recited in Claim 1.

SUGAWARA DOES NOT DISCLOSE OR RENDER OBVIOUS “A PLURALITY OF MAIN ELECTRODES WHICH ARE ELECTRICALLY CONNECTED TO THE PLURALITY OF SECOND SEMICONDUCTOR REGIONS, WHEREIN THE GATE WIRING IS ARRANGED BETWEEN THE MAIN ELECTRODES AND THE GATE WIRING IS SEPARATED FROM THE MAIN ELECTRODES BY A SECOND INSULATING FILM” AS RECITED IN CLAIM 1.

Sugawara describes in FIG. 1, for example, source electrode 11.³ Throughout the description, Sugawara refers to a single source electrode 11. There is no description in Sugawara of “a plurality of main electrodes 11, TS” as asserted in the Office Action at the top of page 4. Rather, Sugawara states “TS is a source terminal”.⁴ Further, Sugawara refers to a single device in stating “a source electrode 11 is formed on the surface of the substrate and a drain electrode 10 is formed on the rear face of the substrate, and an insulated gate semiconductor device (MOSFET) is obtained.”⁵ Thus, there is no description in Sugawara of a plurality of source electrodes and a gate wiring arranged between the source electrodes as recited in Claim 1.

SUGAWARA DOES NOT DISCLOSE OR RENDER OBVIOUS “A FIRST MAIN ELECTRODE WHICH IS DIVIDED INTO A PLURALITY OF FIRST MAIN

¹ Sugawara column 5, lines 57-61 and column 8, lines 41-67.

² Column 5, line 6.

³ Column 6, lines 9-10.

⁴ Column 5, line 5.

⁵ Column 6, lines 1-4.

**ELECTRODE UNITS, THE FIRST MAIN ELECTRODE UNITS BEING
ELECTRICALLY CONNECTED TO THE SECOND SEMICONDUCTOR REGION
AND THE THIRD SEMICONDUCTOR REGION" AS RECITED IN CLAIM 56.**

As pointed out above, Sugawara describes a single source electrode 11 and a single insulated gate semiconductor device (MOSFET). That is, there is no description in Sugawara of "a first main electrode 11 which is divided into a plurality of first main electrode units" as asserted in the Office Action, page 6, lines 12-13.

**SUGAWARA DOES NOT DISCLOSE OR RENDER OBVIOUS "A METAL
GATE WIRING WHICH IS ELECTRICALLY CONNECTED TO THE GATE
ELECTRODE AND WHICH IS ARRANGED BETWEEN THE FIRST MAIN
ELECTRODE UNITS, WHEREIN THE METAL GATE WIRING IS SEPARATED
FROM THE FIRST MAIN ELECTRODE BY A FIRST INSULATING FILM" AS
RECITED IN CLAIM 56.**

As pointed out above, Sugawara describes a gate terminal TG connected to insulated gate electrode 14, and a source electrode 11. There is no description in Sugawara of metal gate wiring arranged between the plurality of first main electrode units as asserted in the Office Action, page 6, lines 15-16. That is, there is no description in Sugawara of gate wiring arranged between the first main electrode units as recited in Claim 56.

**SUGAWARA DOES NOT DISCLOSE OR RENDER OBVIOUS "THE
HIGHEST PORTION OF AN UPPERMOST SURFACE OF THE GATE WIRING IS
NOT HIGHER THAN THE UPPER SURFACES OF THE MAIN ELECTRODES" AS
RECITED IN CLAIM 1.**

The Office Action asserts that "Figure 1 of Sugawara et al. depicts the highest portion of an uppermost surface of the gate wiring Tg is not higher than the upper surfaces of the main electrode Ts." Applicants respectfully disagree.

As shown in Sugawara FIG. 1, for example, gate terminal TG is connected to gate electrode 14 and source terminal TS is connected to source electrode 11. Gate terminal TG and source terminal TS are shown schematically. There is no description in Sugawara of the relative height or physical positions of gate terminal TG and source terminal TS. Therefore, Sugawara neither discloses nor renders obvious the recitation in Claim 1 that the highest portion of an uppermost surface of the gate wiring is not higher than the upper surfaces of the main electrodes. Furthermore, as pointed out above, Sugawara does not describe a plurality of main electrodes.

THE RECITATION IN CLAIMS 1 AND 56 THAT THE “GATE WIRING IS NOT ELECTRICALLY CONNECTED TO THE CONNECTING PLATE” IS DEFINITE AND OPERABLE.

In Applicants’ specification and drawings, for example, FIG. 1, connecting plate 115 is connected to source electrodes 114.⁶ Gap 110a is present between the plurality of source electrodes 114. First gate wiring 104 and second gate wiring 110 are formed between first source electrodes 112. Second gate wiring 110 is surrounded on both sides and the top by second insulating film 113. Second insulating film 113 is further separated from connecting plate 115 by gap 110a. Therefore, the gate wiring is not electrically connected to the

⁶ See specification page 9, line 24 to page 12, line 8.

connecting plate as recited in Claims 1 and 56. Thus, it is respectfully submitted that Claims 1-2, 4-5, 45-47, and 52-69 are definite under 35 U.S.C. § 112, second paragraph, and operable under 35 U.S.C. § 101.

RESPECTFULLY SUBMITTED,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Michael L. Gellner
Registration No. 27,256

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 08/07)

I:\ATTY\MLG\239801US\239801US-AB.DOC